WYJ6 ERRATA

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This documents contains the list of known errors in WYJ6 cards.

Model	Interface	SubVendor	SubId	PCI RevID	Board revision	firmware
WYJ6-V0-R1	BUSMAT	0xff00	0x0001	1	r0	wyj6-0.1
WYJ6-V1-5M-R1	BUSMAT	0xff00	0x0002	1	r1	wyj6-0.1
WYJ6-V1-9M-R1	BUSMAT	0xff00	0x0003	1	r1	wyj6-0.1
WYJ6-V0-R2	BUSMAT	0xff00	0x0001	2	r0	wyj6-0.2
WYJ6-V1-5M-R2	BUSMAT	0xff00	0x0002	2	r1	wyj6-0.2
WYJ6-V1-9M-R2	BUSMAT	0xff00	0x0003	2	r1	wyj6-0.2
WYJ6-V0-R3	BUSMAT	0xff00	0x0001	3	r0	wyj6-0.3
WYJ6-V1-5M-R3	BUSMAT	0xff00	0x0002	3	r1	wyj6-0.3
WYJ6-V1-9M-R3	BUSMAT	0xff00	0x0003	3	r1	wyj6-0.3

1. During Xilinx XL95144XL CPLD initialization (100 μs typical) output buffer is enabled on all SRAM chips. It makes bus unusable in this time. However during CPLD initialization the reset signal is also asserted and as long the host CPU uses bus reset signal no significant problem occurs.

Fix: Fixed in board revision 1.

Affected models: WYJ6-V0-R1, WYJ6-V0-R2

2. The MEMW# signal needed for page-selection based write protection is routed directly to SRAM chips.

Workaround: In some test boards the write protection was emulated using chip select but it caused bigger problems.

Fix: Fixed in board revision 1.

Affected models: WYJ6-V0-R1, WYJ6-V0-R2

3. The card's watchdog is enabled by default and causes asserting RESET signal. For systems that does not use WYJ6 card's watchdog it may cause unwanted bus resets.

Fix: Partially fixed in board revision 1. The watchdog might be effectively disabled by disabling Legacy Mode.

Affected models: WYJ6-V0-R1, WYJ6-V0-R2

4. Writes to higher 16-bits of the Rambat Page Register are ignored and don't affect the rambat write protection timeout. This limits the duration of rambat write unlocked window when 32-bit Rambat Page Register writes are used.

Workaround: Use only 8-bit and 16-bit Rambat Page Register writes.

Fix: Fixed in firmware revision 0.2 (PCI RevisionID 2).

Affected models: WYJ6-V0-R1, WYJ6-V1-5M-R1, WYJ6-V1-9M-R1

5. The writes to PCI Configuration Space, Memory Region 0 and Compatibility I/O Registers requires higher hold time than allowed.

Fix: Fixed in firmware revision 0.2 (PCI RevisionID 2).

Affected models: WYJ6-V0-R1, WYJ6-V1-5M-R1, WYJ6-V1-9M-R1

6. WYJ-6 cards with 9 MiB of memory in the Legacy Mode incorrectly map pages 128 to 255. They should be lower-halfs of pages 128 to 255 but they are mapped to higher-parts, like the higher-parts. Effectively, the pages 128 to 255 are just 16 KiB, not 32 KiB. AR-2c just detects such cards as 4 MiB, not 8 MiB.

Fix: Fixed in firmware revision 0.3 (PCI RevisionID 3).

Affected models: WYJ6-V0-R1, WYJ6-V1-9M-R1, WYJ6-V0-R2, WYJ6-V1-9M-R2