MicroSTER WC-4v5 — User's Manual

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1 Introduction

This is the user's manual for MicroSTER WC-4v5 cards. The WC4v5 card provides 6 digital inputs, an interface for Hitachi HD44780-compatible LCD controllers, an interface for a 6-key keyboard and and interface for two additional keys.

WC-4v5 cards use the BUSMAT bus interface and support autoconfiguration compatible with the ARBus 0.0.

1.1 New revisions

This is the revision 0.0 of this specification. The first number is the major revision number. The major revision number identifies the hardware interface version. Two documentations with the same major revision define the same hardware interface. The second number is the minor revision. This number identifies the version of the documentation of the same hardware interface.

Latest revision of this document is available at `http://www.microster.pl/doc/wc4`.

1.2 Copyright

2 Technical specifications

Bus interface	BUSMAT
Bus frequency	up to 16.7 MHz
Power supply voltage	5 V ±5%
Number of inputs	6
Inputs type	DC
Inputs current flow direction	sink
Inputs voltage	24 V or 110 V
Inputs voltage tolerance	±35%
Inputs current	5 mA to 10 mA
Inputs isolation	≥ 1000 V

3 Parameters

3.1 Absolute Maximum Ratings

Parameter	Min	Max	Unit
Supply voltage	-0.5	6.0	V
Input voltage			
24 V	-5	36	V
110 V	-5	165	V
Storage temperature	-40	85	°C

3.2 Recommended operating conditions

Parameter	Min	Typ	Max	Unit
Supply voltage	4.75	5	5.25	V
Temperature	5		70	°C
Low-level input current	0		0.25	mA
High-level input current	5	6.5	10	mA
Voltage drop		3.3	4.6	V

The voltage drop parameter specifies the voltage drop on non-resistive, non-linear elements.

4 Ordering guide

The WC-4v5 card is available in the following versions:

Model	Bus	No. keys	Input voltage
`WC4-24`	BUSMAT	0	24 V DC
`WC4-110`	BUSMAT	0	110 V DC
`WC4-24P2`	BUSMAT	2	24 V DC
`WC4-110P2`	BUSMAT	2	110 V DC

5 Input/Output signals

5.1 External connector

Pin	Symbol	Description
1	24V	24 V power supply output voltage
2	GND	24 V power supply ground
3	SI2/DI2	Special input 2 / Digital input 2, 24 V
4	24V	24 V output voltage
5	SI3/DI3	Special input 3 / Digital input 3, 24 V
6	DI_GND	Binary inputs 4–7 common ground
7	DI4	Digital input 4, 24 V or 110 V
8	DI5	Digital input 5, 24 V or 110 V
9	DI6	Digital input 6, 24 V or 110 V
10	DI7	Digital input 7, 24 V or 110 V

Digital inputs 2 and 3 have selectable ground by a jumper ground. The power supply or digital inputs ground can be selected.

5.2 24 V output

The WC-4v5 card have built-in 2 Watt 24 V isolated power supply unit designed for powering external components for two special binary inputs 2 and 3.

Parameter	Min	Typ	Max	Unit
Output voltage	21.6	24	34	V
Output current	0		80	mA
Capacitive load			110	μF

Without load the output voltage might be much higher than the nominal 24 V.

6 Configuration

6.1 DI2/DI3 ground selection

The ground for Digital inputs 2 and 3 is selected by J2 and J3 jumpers.

J2	DI2 ground
1-2	Digital inputs ground
2-3	Power supply ground

J3	DI3 ground
1-2	Digital inputs ground
2-3	Power supply ground

6.2 Address selection

The WC-4v5 card ARBus device number can be configured using `ADDR` jumper.

`ADDR`				DevNo	Configuration Memory	Legacy Port
0	0	0	0	0	`0xd8000`	`0xfd82`
0	0	0	1	1	`0xd8800`	`0xfd82`
0	0	1	0	2	`0xd9000`	`0xfd82`
0	0	1	1	3	`0xd9800`	`0xfd82`
0	1	0	0	4	`0xda000`	`0xfd82`
0	1	0	1	5	`0xda800`	`0xfd82`
0	1	1	0	6	`0xdb000`	`0xfd82`
0	1	1	1	7	`0xdb800`	`0xfd82`
1	0	0	0	8	`0xdc000`	`0xfd82`
1	0	0	1	9	`0xdc800`	`0xfd82`
1	0	1	0	10	`0xdd000`	`0xfd82`
1	0	1	1	11	`0xdd800`	`0xfd82`
1	1	0	0	12	`0xde000`	`0xfd82`
1	1	0	1	13	`0xde800`	`0xfd82`
1	1	1	0	14	`0xdf000`	`0xfd82`
1	1	1	1	15	`0xdf800`	`0xfd82`

7 Configuration Registers

The WC-4v5 card have 256-bytes of PCI-compatible Configuration Address Space (see Fig. 1). Access for this address space is usually provided by bus interface driver in operating system. If not see the bus interface specification for information about how to access the Configuration Address Space on your system.

7.1 Vendor ID

Offset	0x00
Width	16 bit
Type	RO
Reset value	0xff00

The Vendor ID identifies the manufacturer of the device. For this device this register is equal to 0xff00.

7.2 Device ID

Offset	0x02
Width	16 bit
Type	RO
Reset value	0x000c

The Device ID identifies the device model. For this device this register is equal to 0x000c.

Offset	3	2	1	0
0x00	Device ID (0x000c)		Vendor ID (0xff00)	
0x04	Status		Command	
0x08	Base Class (0x11)	Sub-class (0x80)	ProgIF (0x00)	Revision ID
0x0c	Reserved	Header Type	Reserved	Reserved
0x10	Base Address Register 0			
0x14–0x2b	Reserved			
0x2c	Subsystem Device ID		Subsystem Vendor ID	
0x30–0x4f	Reserved			
0x50	Reserved			Inputs count (8)
0x54	Reserved		DI32 Command (0x0001)	
0x54–0xef	Reserved			
0xf0	0x53	0x42	0x52	0x41
0xf4-0xff	Reserved			

Figure 1: WC-4v5 Configuration Address Space.

7.3 Command

Offset	0x04
Width	16 bit
Type	RW
Reset value	0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESV														MEM	IO
RO														RW	RO

Command Register Bit Descriptions

Bit	Name	Description
15–2	RESV	**Reserved**.
1	MEM	**Memory Space**. Set to enable decoding of Memory Regions
0	IO	**IO Space**. Always cleared.

7.4 Status

Offset	0x06
Width	16 bit
Type	RO
Reset value	0x0000

The Status register is always equal to 0.

7.5 Revision ID

Offset	0x08
Width	8 bit
Type	RO
Reset value	Implementation specific

The Revision ID identifies the revision of the device.

7.6 ProgIF

Offset	0x09
Width	8 bit
Type	RO
Reset value	0x00

The ProgIF register identifies the programming interface in specified the class of the device. This device reports programming interface as 0x00.

7.7 Sub-class

Offset	0x0a
Width	8 bit
Type	RO
Reset value	0x80

The Sub-class register identifies the sub-class of the device. This device uses class 0x11 and sub-class 0x80 — Signal Processing Controller.

7.8 Base Class

Offset	0x0b
Width	8 bit
Type	RO
Reset value	0x11

The Base Class register identifies the class of the device. This device uses class 0x11 — Signal Processing Controller.

7.9 Header Type

Offset	0x0e
Width	8 bit
Type	RO
Reset value	0x00

The Header Type identifies the type of Configuration Space header.

7.10 Base Address Register 0

Offset	0x10
Width	32 bit
Type	RW
Reset value	0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
RO												RW			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR												P	TYPE		IO
RW												RO		RO	RO

Base Address Register 0 Bit Descriptions

Bit	Name	Description
31–4	ADDR	**Address**. The ADDR sets the bits 31–4 of region 0 base address. Bits 31-20 bits are always cleared to indicate card that supports only 20 address bits. Bits 8-4 are always cleared to indicate 512 byte region.
3	P	**Prefetchable**. Cleared to indicate non-prefetchable region.
2-1	TYPE	**Type**. Always set to 0 — 32-bit base address.
0	IO	**IO Space indicator**. Cleared to indicate Memory Space.

7.11 Subsystem Vendor ID

Offset	0x2c
Width	16 bit
Type	RO
Reset value	Subsystem specific

The Subsystem Vendor ID is assigned by the expansion board or the subsystem vendor.

7.12 Subsystem ID

Offset	0x2e
Width	16 bit
Type	RO
Reset value	Subsystem specific

The Subsystem ID is assigned by the expansion board or the subsystem vendor.

7.13 Inputs count

Offset	0x50
Width	8 bit
Type	RO
Reset value	0x0008

The Inputs count register specifies the number of available digital inputs. For WC-4v5 card it's equal to 8.

7.14 DI32 Command

Offset	0x54
Width	16 bit
Type	RW
Reset value	0x0001

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESV															IO
RO															RW

Command Register Bit Descriptions

Bit	Name	Description
15–1	RESV	**Reserved**.
0	COMPAT	**Compatibility mode**. Set to enable Legacy I/O port decoding.

8 Region 0 — Runtime registers

Runtime Register Summary

Offset	Type	Register	Reset value	Description
0x00	RO	Binary Input Register	—	8.1
0x100	RO	LOKAL Keys	—	8.2
0x101	RW	LOKAL Control	0x80	8.3
0x102	RW	LOKAL Data	0x00	8.4

8.1 Binary Input Register

Offset 0x00
Width 8 bit
Type RO
Reset value —

7	6	5	4	3	2	1	0
DI						KEY1	KEY0
RO						RO	RO

Binary Input Register Bit Descriptions

Bit	Name	Description
7–2	DIn	**Digital Input n value**. The Dn bit shows the negated logical value of n-th input signal. The bit value is equal to 0 if the voltage is applied to digital input. It's equal to 1 otherwise.
1	KEY1	**Key 1**. General purpose key. Optional. The bit value is equal to 0 if the key is pressed. It's equal to 1 otherwise.
0	KEY0	**Key 0**. General purpose key. Optional. The bit value is equal to 0 if the key is pressed. It's equal to 1 otherwise.

8.2 LOKAL Keys

Offset 0x100
Width 8 bit
Type RO
Reset value —

7	6	5	4	3	2	1	0
RESV		MINUS	PLUS	R	E	ENTER	ESC
RO		RO	RO	RO	RO	RO	RO

Control Register Bit Descriptions

Bit	Name	Description
7–6	RESV	**Reserved**. Read as zero.
5	MINUS	**Minus Key**. This bit is set when the Minus Key is pressed; it's cleared otherwise.
4	PLUS	**Plus Key**. This bit is set when the Plus Key is pressed; it's cleared otherwise.
3	E	**'E' Key**. This bit is set when the 'E' Key is pressed; it's cleared otherwise.
2	R	**'R' Key**. This bit is set when the 'R' Key is pressed; it's cleared otherwise.
1	ENTER	**Enter Key**. This bit is set when the Enter Key is pressed; it's cleared otherwise.
0	ESC	**Escape Key**. This bit is set when the Escape Key is pressed; it's cleared otherwise.

8.3 LOKAL Control

Offset	0x101
Width	8 bit
Type	RW
Reset value	0x80

7	6	5	4	3	2	1	0
OD	RESV				E	RW	RS
RW	RO				RW	RW	RW

Control Register Bit Descriptions

Bit	Name	Description
7	OD	**Output Disable**. Setting this bit disables the LCD Display Data bus drivers.
6-3	RESV	**Reserved**. Read as zero controller.
2	E	**E**. The E pin of the LCD display controller.
1	RW	**RW**. The RW pin of the LCD display controller.
0	RS	**RS**. The RS pin of the LCD display controller.

The WC-4v5 card has a static protection against enabling both data bus output buffers in the WC-4v5 chip by clearing **Output Disable** bit and the LCD Controller by setting the **RW** bit. So the WC-4v5 guarantees that in the steady state both data buffers are never enabled. However, the WC-4v5 controller does not guarantee the necessary safe time period between disabling one buffer and enabling the other. To avoid possible short periods, when both buffers are enabled, it's recommended to disable the output enable on one side before enabling it on the other side.

8.4 LOKAL Data

Offset	0x102
Width	8 bit
Type	RW
Reset value	0x00

7	6	5	4	3	2	1	0
DATA							
RW							

Control Register Bit Descriptions

Bit	Name	Description
7-0	DATA	**Data Bus**. The LCD display controller data bus. The output enable is controlled by the **Output Disable** bit in the LOKAL Control register (8.3).

9 Legacy registers

The WC-4v5 card provides following Legacy I/O port registers:

Runtime Register Summary

Offset	Type	Register	Reset value	Description
0xfd82	RO	Binary Input Register	—	8.1

A Card revisions

Vendor ID	Device ID	Subsystem Vendor ID	Subsystem ID	Model
0xffff	0x000c	0xffff	0x000a	24 V
0xffff	0x000c	0xffff	0x000b	110 V