# DI32 — Programing Interface rev. 1.0

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## 1 Introduction

This document describes the programing interface of the DI32 digital inputs controller. The DI32 supports up to 32 digital inputs.

This programming interface is designed to use with PCI-compatible buses, including PCI, PCI-X, PCI Express, PCI/104 and ARBus.

### 1.1 New revisions

This is the revision 1.0 of this specification. The first number is the major revision number. The major revision number identifies the hardware interface version. Two documentations with the same major revision define the same hardware interface. The second number is the minor revision. This number identifies the version of the documentation of the same hardware interface.

Latest revision of this document is available at `http://www.microster.pl/doc/di32`.

### 1.2 Revision History

Revision 1.0 added Runtime Registers accessible via Memory region configured by Base Address Register 0.

### 1.3 Copyright



## 2 Configuration Registers

The DI32 controller have 256-bytes of PCI-compatible Configuration Address Space (see Fig. 1). Access for this address space is usually provided by bus interface driver in operating system. If not see the bus interface specification for information about how to access the Configuration Address Space on your system.

### 2.1 Vendor ID

| | |
|---|---|
| Offset | 0x00 |
| Width | 16 bit |
| Type | RO |
| Reset value | 0xff00 |

The Vendor ID identifies the manufacturer of the device. For this device this register is equal to 0xff00.

### 2.2 Device ID

| | |
|---|---|
| Offset | 0x02 |
| Width | 16 bit |
| Type | RO |
| Reset value | 0x0001 |

The Device ID identifies the device model. For this device this register is equal to 0x0001.

[1] This signature at 0xf0 is used only devices using ARBus bus interface. For devices using other interfaces this area is reserved.

| Offset | 3 | 2 | 1 | 0 |
|---|---|---|---|---|
| 0x00 | Device ID (0x0001) | | Vendor ID (0xff00) | |
| 0x04 | Status | | Command | |
| 0x08 | Base Class (0x11) | Sub-class (0x80) | ProgIF (0x00) | Revision ID |
| 0x0c | Reserved | Header Type | Reserved | Reserved |
| 0x10–0x2b | Reserved | | | |
| 0x2c | Subsystem Device ID | | Subsystem Vendor ID | |
| 0x30–0x3f | Reserved | | | |
| 0x40 | Binary Input Register | | | |
| 0x44–0xef | Reserved | | | |
| 0xf0[1] | 0x53 | 0x42 | 0x52 | 0x41 |
| 0xf4-0xff | Reserved | | | |

Figure 1: DI32 Configuration Address Space.

## 2.3 Command

| | |
|---|---|
| Offset | 0x04 |
| Width | 16 bit |
| Type | RW |
| Reset value | 0x0000 |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESV | | | | | | | | | | | | | | MEM | IO |
| RO | | | | | | | | | | | | | | RW | RO |

Command Register Bit Descriptions

| Bit | Name | Description |
|---|---|---|
| 15–2 | RESV | **Reserved**. |
| 1 | MEM | **Memory Space**. Set to enable decoding of Memory Regions |
| 0 | IO | **IO Space**. Unused, always equal to zero. Memory Space |

## 2.4 Status

| | |
|---|---|
| Offset | 0x06 |
| Width | 16 bit |
| Type | RO |
| Reset value | 0x0000 |

The Status register is always equal to 0.

## 2.5 Revision ID

| | |
|---|---|
| Offset | 0x08 |
| Width | 8 bit |
| Type | RO |
| Reset value | 0x01 |

The Revision ID identifies the revision of the device. For this revision this register is equal to 1.

## 2.6 ProgIF

| | |
|---|---|
| Offset | 0x09 |
| Width | 8 bit |
| Type | RO |
| Reset value | 0x00 |

The ProgIF register identifies the programming interface in specified class of device. This device reports programming interface as 0x00.

## 2.7 Sub-class

| | |
|---|---|
| Offset | 0x0a |
| Width | 8 bit |
| Type | RO |
| Reset value | 0x80 |

The Sub-class register identifies the sub-class of device. This device uses class 0x11 and sub-class 0x80 — Signal Processing Controller.

## 2.8 Base Class

| | |
|---|---|
| Offset | 0x0b |
| Width | 8 bit |
| Type | RO |
| Reset value | 0x11 |

The Base Class register identifies the class of device. This device uses class 0x11 — Signal Processing Controller.

## 2.9 Header Type

| | |
|---|---|
| Offset | 0x0e |
| Width | 8 bit |
| Type | RO |
| Reset value | 0x00 or 0x80 |

The Header Type identifies the type of Configuration Space header. This field is equal to 0x00 in single function devices or 0x80 in multifunction devices.

## 2.10 Base Addres Register 0

Note: This subsection describes 32-bit Base Address Register. Some impementations may support 64-bit Base Address Registers and such register will occupy two words. See PCI Specification for detailed description of Base Address Registers.

| | |
|---|---|
| Offset | 0x10 |
| Width | 32 bit |
| Type | RW |
| Reset value | implementation specific |

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ADDR | | | | | | | | | | | | | | | |
| RW | | | | | | | | | | | | | | | |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ADDR | | | | | | | | | | | | P | TYPE | | IO |
| RW | | | | RO | | | | | | | | RO | RO | | RO |

Base Address Register 0 Bit Descriptions

| Bit | Name | Description |
|---|---|---|
| 31–4 | ADDR | **Address**. The ADDR sets the bits 31–4 of region 0 base address. Note that on some buses like ARBus the address may be limitted and higher bits are always cleared. Some lower bits may be also cleared to reduce size of address decoder. In such case the memory region is larger than minimal 16 bytes used by DI32 interface. Accessing addresses above 16 have an impementation-specific behaviour. |
| 3 | P | **Prefetchable**. implementation specific |
| 2-1 | TYPE | **Type**. implementation specific, 0 (32-bit base address) is asummed in this documentation |
| 0 | IO | **IO Space indicator**. cleared to indicate Memory Space |

## 2.11 Subsystem Vendor ID

| | |
|---|---|
| Offset | 0x2c |
| Width | 16 bit |
| Type | RO |
| Reset value | Subsystem specific |

The Subsystem Vendor ID is assigned by expansion board or subsystem vendor.

## 2.12 Subsystem ID

| | |
|---|---|
| Offset | 0x2e |
| Width | 16 bit |
| Type | RO |
| Reset value | Subsystem specific |

The Subsystem ID is assigned by expansion board or subsystem vendor.

## 2.13 Binary Input Register

| | |
|---|---|
| Offset | 0x40 |
| Width | 32 bit |
| Type | RO |
| Reset value | — |

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D31 | D30 | D29 | D28 | D27 | D26 | D25 | D24 | D23 | D22 | D21 | D20 | D19 | D18 | D17 | D16 |
| RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO |

Binary Input Register Bit Descriptions

| Bit | Name | Description |
|---|---|---|
| 31–0 | Dn | **Digital Input n value**. The Dn bit shows the negated logical value of n-th input signal. The bit value is equal to 0 if the voltage is applied to digital input. It's equal to 1 otherwise. |

# 3 Runtime registers

Runtime Register Summary

| Offset | Type | Register | Reset value | Description |
|---|---|---|---|---|
| 0x0 | RO | Binary Input Register | | 3.1 |

## 3.1 Binary Input Register

| | |
|---|---|
| Offset | 0x40 |
| Width | 32 bit |
| Type | RO |
| Reset value | — |

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D31 | D30 | D29 | D28 | D27 | D26 | D25 | D24 | D23 | D22 | D21 | D20 | D19 | D18 | D17 | D16 |
| RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO |

Binary Input Register Bit Descriptions

| Bit | Name | Description |
|---|---|---|
| 31–0 | Dn | **Digital Input n value**. The Dn bit shows the negated logical value of n-th input signal. The bit value is equal to 0 if the voltage is applied to digital input. It's equal to 1 otherwise. |