# DI32 — User's manual

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## Features

- 16 or 32 isolated binary inputs
- 24 V or 110 V input voltage
- PC/104 bus
- AR4C form factor

## 1 Introduction

### 1.1 New revisions

This is the revision 2.0 of this specification. The first number is the major revision number. The major revision number identifies the hardware revision. The second number is the minor revision. This number identifies the version of the documentation of for the same hardware.

Latest revision of this document is available at `http://www.microster.pl/doc/di32`.

### 1.2 Copyright



## 2 Technical specifications

| | |
|---|---|
| Bus interface | PC/104 |
| Bus frequency | up to 16.7 MHz |
| Form factor | AR4C |
| Power supply voltage | 5 V ±5% |
| Power supply current | up to 75 mA |
| Dimensions [mm] | 151×125×19 |
| Number of inputs | 16 or 32 |
| Inputs type | DC |
| Inputs current flow direction | sink |
| Inputs voltage | 24 V or 110 V |
| Inputs voltage tolerance | ±35% |
| Inputs current | 1.3 mA to 6 mA |
| Inputs isolation | ≥ 1000 V |

## 3 Digital inputs

The DI32 card have 4 or 8 groups of binary signals (see Fig. 1). Cards with 16 inputs does not have groups 4–7.

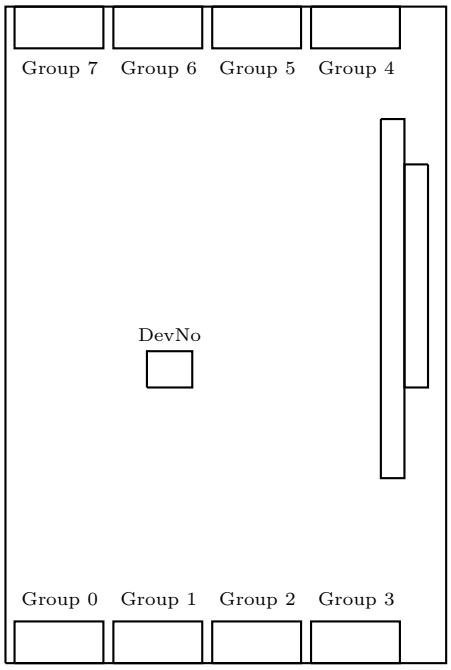


Figure 1: DI32 card input connectors.

Each group have 4 signals $B_0$–$B_3$ with common ground (see Fig. 2). Card does not provide isolation between pins within a group.

| 1 | 2 | 3 | 4 | 5 |
|---|---|---|---|---|
| GND | $B_0$ | $B_1$ | $B_2$ | $B_3$ |

Figure 2: DI32 connector.

# 4 Card configuration

The DI32 card is configured by a single DevNo switch which selects the ARBus device number. Each ARBus device must have unique number on a single PC/104 bus. The device number selects the PCI-like Configuration Memory Base address:

| DevNo | Configuration Memory address |
|---|---|
| 0 | `0xd8000` |
| 1 | `0xd8800` |
| 2 | `0xd9000` |
| ⋮ | ⋮ |
| 8 | `0xdc000` |
| 9 | `0xdc800` |

# 5 Parameters

## 5.1 Absolute Maximum Ratings

| Parameter | Min | Max | Unit |
|---|---|---|---|
| Supply voltage | -0.5 | 6.0 | V |
| Input voltage | | | |
| 24 V | -30 | 60 | V |
| 110 V | -150 | 300 | V |
| Storage temperature | -40 | 85 | °C |

## 5.2 Recommended operating conditions

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Supply voltage | 4.75 | 5 | 5.25 | V |
| Temperature | 5 | | 70 | °C |
| Low-level input current | 0 | | 0.5 | mA |
| High-level input current | 1.3 | 2 | 6 | mA |
| Voltage drop | | 3.3 | 4.3 | V |

The voltage drop parameter specifies the voltage drop on non-resistive, non-linear elements.

## 5.3 Binary input parameters

| Parameter | 24 V card | | | 110 V card | | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max | |
| R resistors | | 4.7 | | | 24 | | kΩ |
| C capacitor | | 100 | | | 22 | | nF |
| Input resistance | 4.2 | 9.4 | 10.3 | 21 | 48 | 53 | kΩ |
| Isolation voltage | 1000 | | | 1000 | | | V |
| Off–On delay | | 290 | 1000 | | 260 | 1000 | $\mu$s |
| On–Off delay (Off — 0V) | | 300 | 2000 | | 400 | 2000 | $\mu$s |
| On–Off delay (Off — Open) | | 750 | 2000 | | 800 | 2000 | $\mu$s |

# 6 Ordering guide

The DI32 card is available in the following versions:

| Model | Bus | No. Inputs | Input voltage |
|---|---|---|---|
| `DI16-24` | PC/104 | 16 | 24 V DC |
| `DI16-110` | PC/104 | 16 | 110 V DC |
| `DI32-24` | PC/104 | 32 | 24 V DC |
| `DI32-110` | PC/104 | 32 | 110 V DC |

DI32 cards are available also for other non-standard input voltage ranges. The minimal recommended voltage is 8 V and it's is limited by voltage drop parameter. The maximal recommended voltage is 150 V

and it's limited by heat dissipation on resistors related to high-level input current. For higher voltages external resistors are recommended.

# 7 Host interface

The DI32 card uses the PC/104 bus for communication with the host. The card is visible from the bus as two memory regions:

1. 256 bytes of PCI-compatible configuration memory at address `0xd8000 + no * 0x800`, where *no* is the selected ARBus device number.
2. 256 bytes of control registers, the address is configurable by host using the Base Address Register 0 in the PCI configuration header.

## 7.1 Configuration Registers

The DI32 controller have 256-bytes of PCI-compatible Configuration Address Space (see Fig. 3). Access for this address space is usually provided by the bus interface driver in the operating system. If not the Configuration Memory can accessed directly as Memory Mapped I/O at appropriate address (see section 4).

Configuration Register Summary

| Offset | Type | Register | Reset value | Description |
|---|---|---|---|---|
| 0x0 | RO | VendorID | `0xff00` | 7.1.1 |
| 0x2 | RO | DeviceID | `0x0001` | 7.1.2 |
| 0x4 | RW | Command | `0x0000` | 7.1.3 |
| 0x6 | RO | Status | `0x0000` | 7.1.4 |
| 0x8 | RO | RevisionID | `0x02` | 7.1.5 |
| 0x9 | RO | ProgIF | `0x00` | 7.1.6 |
| 0xa | RO | Sub-class | `0x80` | 7.1.7 |
| 0xb | RO | Base Class | `0x11` | 7.1.8 |
| 0xe | RO | Header Type | `0x00` | 7.1.9 |
| 0x10 | RW | BAR0 | `0x00000000` | 7.1.10 |
| 0x2c | RO | SubsystemVendorID | `0xff00` | 7.1.11 |
| 0x2e | RO | SubsystemID | – | 7.1.12 |
| 0x40 | RO | Binary Inputs Register | – | 7.1.13 |

Fig. 3 shows the PCI-compatible configuration memory. The host interface is described in *DI32 — Programming Interface rev 1.0*[1].

### 7.1.1 Vendor ID

| | |
|---|---|
| Offset | 0x00 |
| Width | 16 bit |
| Type | RO |
| Reset value | 0xff00 |

The Vendor ID identifies the manufacturer of the device. For this device this register is equal to 0xff00.

| Offset | 3 | 2 | 1 | 0 |
|---|---|---|---|---|
| 0x00 | Device ID (0x0001) | | Vendor ID (0xff00) | |
| 0x04 | Status | | Command | |
| 0x08 | Base Class (0x11) | Sub-class (0x80) | ProgIF (0x00) | Revision ID (0x02) |
| 0x0c | Reserved | Header Type (0x00) | Reserved | Reserved |
| 0x10 | Base Address Register 0 | | | |
| 0x14–0x3f | Reserved | | | |
| 0x2c | Subsystem Device ID | | Subsystem Vendor ID (0xff00) | |
| 0x30–0x3f | Reserved | | | |
| 0x40 | Binary inputs | | | |
| 0x44–0x4f | Reserved | | | |
| 0x50 | Inputs count | Reserved | | |
| 0x54–0xef | Reserved | | | |
| 0xf0 | 0x53 | 0x42 | 0x52 | 0x41 |
| 0xf4-0xff | Reserved | | | |

Figure 3: DI32 card PCI configuration memory map.

### 7.1.2 Device ID

| | |
|---|---|
| Offset | 0x02 |
| Width | 16 bit |
| Type | RO |
| Reset value | 0x0001 |

The Device ID identifies the device model. For this device this register is equal to 0x0001.

### 7.1.3 Command

| | |
|---|---|
| Offset | 0x04 |
| Width | 16 bit |
| Type | RW |
| Reset value | 0x0000 |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESV | | | | | | | | | | | | | | MEM | IO |
| RO | | | | | | | | | | | | | | RW | RO |

Command Register Bit Descriptions

| Bit | Name | Description |
|---|---|---|
| 15–2 | RESV | **Reserved**. |
| 1 | MEM | **Memory Space**. Set to enable decoding of Memory Regions |
| 0 | IO | **IO Space**. Unused, always equal to zero. Memory Space |

#### 7.1.4 Status

| | |
|---|---|
| Offset | 0x06 |
| Width | 16 bit |
| Type | RO |
| Reset value | 0x0000 |

The Status register is always equal to 0.

#### 7.1.5 Revision ID

| | |
|---|---|
| Offset | 0x08 |
| Width | 8 bit |
| Type | RO |
| Reset value | 0x01 |

The Revision ID identifies the revision of the device. For this revision this register is equal to 1.

#### 7.1.6 ProgIF

| | |
|---|---|
| Offset | 0x09 |
| Width | 8 bit |
| Type | RO |
| Reset value | 0x00 |

The ProgIF register identifies the programming interface in specified class of device. This device reports programming interface as 0x00.

#### 7.1.7 Sub-class

| | |
|---|---|
| Offset | 0x0a |
| Width | 8 bit |
| Type | RO |
| Reset value | 0x80 |

The Sub-class register identifies the sub-class of device. This device uses class 0x11 and sub-class 0x80 — Signal Processing Controller.

#### 7.1.8 Base Class

| | |
|---|---|
| Offset | 0x0b |
| Width | 8 bit |
| Type | RO |
| Reset value | 0x11 |

The Base Class register identifies the class of device. This device uses class 0x11 — Signal Processing Controller.

#### 7.1.9 Header Type

| | |
|---|---|
| Offset | 0x0e |
| Width | 8 bit |
| Type | RO |
| Reset value | 0x00 or 0x80 |

The Header Type identifies the type of Configuration Space header. This field is equal to 0x00 in single function devices or 0x80 in multifunction devices.

#### 7.1.10 Base Address Register 0

| | |
|---|---|
| Offset | 0x10 |
| Width | 32 bit |
| Type | RW |
| Reset value | 0x00000000 |

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ADDR | | | | | | | | | | | | | | | |
| RO | | | | | | | | | | | | RW | | | |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ADDR | | | | | | | | | | | | P | TYPE | | IO |
| RW | | | | | | | | RO | | | | RO | RO | | RO |

Base Address Register 0 Bit Descriptions

| Bit | Name | Description |
|---|---|---|
| 31–4 | ADDR | **Address**. The ADDR sets the bits 31–4 of region 0 base address. Bits 7–0 are hard-wired to zero indicate 256 byte region. The bits 31–20 are hard-wired to zero to indicate 20-bit address bus. |
| 3 | P | **Prefetchable**. Cleared to indicate non-prefetchable memory region. |
| 2-1 | TYPE | **Type**. Set to 0, 32-bit memory region. 0 (32-bit base address) is asummed in this documentation |
| 0 | IO | **IO Space indicator**. Cleared to indicate Memory Space. |

### 7.1.11 Subsystem Vendor ID

| | |
|---|---|
| Offset | 0x2c |
| Width | 16 bit |
| Type | RO |
| Reset value | 0xff00 |

The Subsystem Vendor ID is assigned by expansion board or subsystem vendor. For this device this register is equal to 0xff00.

### 7.1.12 Subsystem ID

| | |
|---|---|
| Offset | 0x2e |
| Width | 16 bit |
| Type | RO |
| Reset value | Model specific |

The SubsystemID depends on card model:

| Model | SubsystemID |
|---|---|
| DI16-V1-24 | 0x0004 |
| DI16-V1-110 | 0x0003 |
| DI32-V1-24 | 0x0002 |
| DI32-V1-110 | 0x0001 |

### 7.1.13 Binary Input Register

| | |
|---|---|
| Offset | 0x40 |
| Width | 32 bit |
| Type | RO |
| Reset value | — |

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D31 | D30 | D29 | D28 | D27 | D26 | D25 | D24 | D23 | D22 | D21 | D20 | D19 | D18 | D17 | D16 |
| RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO |

Binary Input Register Bit Descriptions

| Bit | Name | Description |
|---|---|---|
| 31–0 | Dn | **Digital Input n value**. The Dn bit shows the negated logical value of n-th input signal. The bit value is equal to 0 if the voltage is applied to digital input. It's equal to 1 otherwise. |

## 7.2 Runtime registers

Runtime Register Summary

| Offset | Type | Register | Reset value | Description |
|---|---|---|---|---|
| 0x0 | RO | Binary Input Register | | 7.2.1 |

### 7.2.1 Binary Input Register

| | |
|---|---|
| Offset | 0x40 |
| Width | 32 bit |
| Type | RO |
| Reset value | — |

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D31 | D30 | D29 | D28 | D27 | D26 | D25 | D24 | D23 | D22 | D21 | D20 | D19 | D18 | D17 | D16 |
| RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO |

Binary Input Register Bit Descriptions

| Bit | Name | Description |
|---|---|---|
| 31–0 | Dn | **Digital Input n value**. The Dn bit shows the negated logical value of n-th input signal. The bit value is equal to 0 if the voltage is applied to digital input. It's equal to 1 otherwise. |

# References

[1] Krzysztof Mazur, *DI32 — Programming Interface rev 1.0*, 2013, available online at http://www.microster.pl/doc/di32/di32.pdf